WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising: a plurality of memory cells; paired bit lines connected to the plurality of memory cells; a plurality of precharge circuits for precharging the paired bit lines to a predetermined precharge voltage in accordance with a first control signal; and a bit line precharge voltage generation unit for supplying a voltage for precharging to the plurality of precharge circuits, an equalizing voltage of the paired bit lines being different from the precharge voltage,

the bit line precharge voltage generation unit comprising:

a precharge voltage generation circuit for generating the precharge voltage and supplying the precharge voltage to the plurality of precharge circuits; and

a precharge voltage pumping circuit including a pumping capacitor, a first switch for connecting a first electrode of the pumping capacitor to a first power source, a second switch for connecting the first electrode to an output node of the precharge voltage generation circuit, a third switch for connecting a second electrode of the pumping capacitor to the first power source, a fourth switch for connecting the second electrode to a second power source, and a control circuit for controlling on/off of the first, second, third, and fourth switches.

2. The semiconductor memory device according to claim 1, wherein the first, second, third, and fourth switches and the pumping capacitor are composed of MOS transistors.

3. The semiconductor memory device according to claim 1, wherein the semiconductor memory device has a plurality of gate oxide film thicknesses, and the first, second, third, and fourth switches and the pumping capacitor are composed of MOS transistors with a thick gate oxide film thickness.

4. The semiconductor memory device according to claim 1, wherein the semiconductor memory device has a plurality of gate oxide film thicknesses, and the first, second, third, and fourth switches and the pumping capacitor are composed of MOS transistors with a thin gate oxide film thickness.

5. The semiconductor memory device according to claim 1, wherein the

control circuit of the precharge voltage pumping circuit controls the second switch and the third switch so as to turn them on during precharge or during a predetermined period of time from a commencement of precharge, and controls the first switch and the fourth switch so as to turn them on during the other period of time.

6. The semiconductor memory device according to claim 1, wherein the first control signal is a bit line precharge starting signal to the precharge circuit.

7. The semiconductor memory device according to claim 1, wherein the semiconductor memory device has a first well region of an N-channel MOS transistor and a second well region of a P-channel MOS transistor, and a MOS transistor constituting the pumping capacitor is a transistor in the second well region.

8. The semiconductor memory device according to claim 1, wherein the semiconductor memory device has a triple-well region including a first well region of an N-channel MOS transistor, a second well region of a P-channel MOS transistor, and a third well region of an N-channel MOS transistor, and a MOS transistor constituting the pumping capacitor is a transistor in the third well region.

9. The semiconductor memory device according to claim 1, wherein the first electrode of the pumping capacitor is composed of a gate electrode of a MOS transistor, and the second electrode is composed of a source, a drain, and a substrate of a MOS transistor connected to each other.

10. The semiconductor memory device according to claim 1, wherein the first electrode of the pumping capacitor is composed of a source, a drain, and a substrate of a MOS transistor connected to each other, and the second electrode is composed of a gate electrode of a MOS transistor.

11. The semiconductor memory device according to claim 1, wherein the pumping capacitor uses a plurality of wiring layers in the semiconductor memory device as electrodes, and is composed of capacitance formed between the wiring layers.

12. The semiconductor memory device according to claim 1, wherein the plurality of memory cells are formed in a plurality of memory cell array blocks capable of being activated individually, and the precharge voltage pumping circuit is disposed so as to be paired with each of the memory cell array blocks.

13. The semiconductor memory device according to claim 1, wherein the plurality of memory cells are formed in a plurality of memory cell array blocks capable of being activated individually, and the precharge voltage pumping circuit is disposed so as to be paired with each of the memory cell array blocks and is operated in accordance with a transition from a non-precharged state to a precharged state of each of the memory cell array blocks.

14. The semiconductor memory device according to claim 1, wherein the plurality of memory cells are formed in a plurality of memory cell array blocks capable of being activated individually, and the precharge voltage pumping circuit is disposed so as to be paired with each of the memory cell array blocks and is operated based on a bit line precharge starting signal to the precharge circuit in the memory cell array block.

15. The semiconductor memory device according to claim 12, wherein the bit line precharge voltage generation unit is disposed on one side of the memory cell array block so as to be in parallel with a sense amplifier string.

16. The semiconductor memory device according to claim 12, wherein the bit line precharge voltage generation unit is disposed on one side of the memory cell array block so as to be adjacent to the precharge circuit string.

17. The semiconductor memory device according to claim 12, wherein the bit line precharge voltage generation unit is disposed on one side of the memory cell array block so as to be placed in a row decoder block or so as to be in parallel with a row decoder string.

18. The semiconductor memory device according to claim 12, wherein the bit line precharge voltage generation unit is disposed on one side of the memory cell array block so as to be opposed to a row decoder block with the memory

cell array block interposed therebetween.

19. A semiconductor memory device, comprising: a plurality of memory cells; paired bit lines connected to the plurality of memory cells; a plurality of precharge circuits for precharging the paired bit lines to a predetermined precharge voltage in accordance with a first control signal; and a bit line precharge voltage generation unit for supplying a voltage for precharging to the plurality of precharge circuits, an equalizing voltage of the paired bit lines being different from the precharge voltage,

the bit line precharge voltage generation unit comprising:

a precharge voltage generation circuit for generating the precharge voltage and supplying the precharge voltage to the plurality of precharge circuits; and

a precharge voltage pumping circuit including a pumping capacitor, a first switch for connecting a first electrode of the pumping capacitor to a first power source, a second switch for connecting the first electrode to an output node of the precharge voltage generation circuit, and a control circuit for controlling on/off of the first and second switches, wherein a second electrode of the pumping capacitor is driven with a second control signal.

20. The semiconductor memory device according to claim 19, wherein the first control signal is a bit line precharge starting signal to the precharge circuit.

21. The semiconductor memory device according to claim 19, wherein the first control signal also functions as the second control signal.

22. The semiconductor memory device according to claim 19, wherein the first and second switches and the pumping capacitor are composed of MOS transistors.

23. The semiconductor memory device according to claim 19, wherein the semiconductor memory device has a plurality of gate oxide film thicknesses, and the first and second switches and the pumping capacitor are composed of MOS transistors with a thick gate oxide film thickness.

24. The semiconductor memory device according to claim 19, wherein the

semiconductor memory device has a plurality of gate oxide film thicknesses, and the first and second switches and the pumping capacitor are composed of MOS transistors with a thin gate oxide film thickness.

25. The semiconductor memory device according to claim 19, wherein the control circuit of the precharge voltage pumping circuit controls the second switch so as to turn it on with the first control signal during precharge or during a predetermined period of time from a commencement of precharge, and is operated so that charge in the pumping capacitor is transferred to an output node of the precharge voltage generation circuit with the second control signal.

26. The semiconductor memory device according to claim 19, wherein the semiconductor memory device has a first well region of an N-channel MOS transistor and a second well region of a P-channel MOS transistor, and a MOS transistor constituting the pumping capacitor is a transistor in the second well region.

27. The semiconductor memory device according to claim 19, wherein the semiconductor memory device has a triple-well region including a first well region of an N-channel MOS transistor, a second well region of a P-channel MOS transistor, and a third well region of an N-channel MOS transistor, and a MOS transistor constituting the pumping capacitor is a transistor in the third well region.

28. The semiconductor memory device according to claim 19, wherein the first electrode of the pumping capacitor is composed of a gate electrode of a MOS transistor, and the second electrode is composed of a source, a drain, and a substrate of a MOS transistor connected to each other.

29. The semiconductor memory device according to claim 19, wherein the first electrode of the pumping capacitor is composed of a source, a drain, and a substrate of a MOS transistor connected to each other, and the second electrode is composed of a gate electrode of a MOS transistor.

30. The semiconductor memory device according to claim 19, wherein the pumping capacitor uses a plurality of wiring layers in the semiconductor

memory device as electrodes, and is composed of capacitance formed between the wiring layers.

31. The semiconductor memory device according to claim 19, wherein the plurality of memory cells are formed in a plurality of memory cell array blocks capable of being activated individually, and the precharge voltage pumping circuit is disposed so as to be paired with each of the memory cell array blocks.

32. The semiconductor memory device according to claim 19, wherein the plurality of memory cells are formed in a plurality of memory cell array blocks capable of being activated individually, and the precharge voltage pumping circuit is disposed so as to be paired with each of the memory cell array blocks and is operated in accordance with a transition from a non-precharged state to a precharged state of each of the memory cell array blocks.

33. The semiconductor memory device according to claim 19, wherein the plurality of memory cells are formed in a plurality of memory cell array blocks capable of being activated individually, and the precharge voltage pumping circuit is disposed so as to be paired with each of the memory cell array blocks and is operated based on a bit line precharge starting signal to the precharge circuit in the memory cell array block.

34. The semiconductor memory device according to claim 31, wherein the bit line precharge voltage generation unit is disposed on one side of the memory cell array block so as to be in parallel with a sense amplifier string.

35. The semiconductor memory device according to claim 31, wherein the bit line precharge voltage generation unit is disposed on one side of the memory cell array block so as to be adjacent to the precharge circuit string.

36. The semiconductor memory device according to claim 31, wherein the bit line precharge voltage generation unit is disposed on one side of the memory cell array block so as to be placed in a row decoder block or so as to be in parallel with a row decoder string.

37. The semiconductor memory device according to claim 31, wherein the bit line precharge voltage generation unit is disposed on one side of the memory cell array block so as to be opposed to a row decoder block with the memory cell array block interposed therebetween.

38. The semiconductor memory device according to claim 19, wherein a voltage amplitude of the second control signal is substantially the same as a voltage amplitude of a word line connected to the plurality of memory cells.

39. A semiconductor memory device, comprising: a plurality of memory cells; paired bit lines connected to the plurality of memory cells; a plurality of precharge circuits for precharging the paired bit lines to a predetermined precharge voltage in accordance with a first control signal; and a bit line precharge voltage generation unit for supplying a voltage for precharging to the plurality of precharge circuits, an equalizing voltage of the paired bit lines being different from the precharge voltage,

the bit line precharge voltage generation unit comprising:

a precharge voltage generation circuit for generating the precharge voltage and supplying the precharge voltage to the plurality of precharge circuits; and

a precharge voltage pumping circuit including a pumping capacitor, a first switch for connecting a first electrode of the pumping capacitor to a first power source, a second switch for connecting the first electrode to an output node of the precharge voltage generation circuit, and a control circuit for controlling on/off of the first and second switches, wherein a second electrode of the pumping capacitor is driven with a second control signal,

wherein the second control signal rises during an activation period of a first control signal that is a bit line precharge starting signal to the precharge circuit.

40. A semiconductor memory device, comprising: a plurality of memory cells; paired bit lines connected to the plurality of memory cells; a plurality of precharge circuits for precharging the paired bit lines to a predetermined precharge voltage in accordance with a first control signal; and a bit line precharge voltage generation unit for supplying a voltage for precharging to the plurality of precharge circuits, an equalizing voltage of the paired bit lines being different from the precharge voltage,

the bit line precharge voltage generation unit comprising:

a precharge voltage generation circuit for generating the precharge voltage and supplying the precharge voltage to the plurality of precharge circuits; and

a precharge voltage pumping circuit including a pumping capacitor, a first switch for connecting a first electrode of the pumping capacitor to a first power source, a second switch for connecting the first electrode to an output node of the precharge voltage generation circuit, a control circuit for controlling on/off of the first and second switches, and a precharge voltage pumping circuit for driving a second electrode of the pumping capacitor with a second control signal,

wherein the second control signal rises with a transition time longer than a transition time of the first control signal, after a predetermined delay time from activation of the first control signal that is a bit line precharge starting signal to the precharge circuit.

41. A semiconductor device with a semiconductor memory device and a logic circuit device therein,

wherein the semiconductor memory device includes: a plurality of memory cells; paired bit lines connected to the plurality of memory cells; a plurality of precharge circuits for precharging the paired bit lines to a predetermined precharge voltage in accordance with a first control signal; and a bit line precharge voltage generation unit for supplying a voltage for precharging to the plurality of precharge circuits, an equalizing voltage of the paired bit lines being different from the precharge voltage,

the bit line precharge voltage generation unit includes:

a precharge voltage generation circuit for generating the precharge voltage and supplying the precharge voltage to the plurality of precharge circuits; and

a precharge voltage pumping circuit including a pumping capacitor, a first switch for connecting a first electrode of the pumping capacitor to a first power source, a second switch for connecting the first electrode to an output node of the precharge voltage generation circuit, a control circuit for controlling on/off of the first and second switches, and a precharge voltage pumping circuit for driving a second electrode of the pumping capacitor with a second control signal, and

a voltage amplitude of the second control signal is substantially the

same as a voltage amplitude of a signal in the logic circuit device.

42. A semiconductor device with a semiconductor memory device and a logic circuit device therein,

wherein the semiconductor memory device includes: a plurality of memory cells; paired bit lines connected to the plurality of memory cells; a plurality of precharge circuits for precharging the paired bit lines to a predetermined precharge voltage in accordance with a first control signal; and a bit line precharge voltage generation unit for supplying a voltage for precharging to the plurality of precharge circuits, an equalizing voltage of the paired bit lines being different from the precharge voltage,

the bit line precharge voltage generation unit includes:

a precharge voltage generation circuit for generating the precharge voltage and supplying the precharge voltage to the plurality of precharge circuits; and

a precharge voltage pumping circuit including a pumping capacitor, a first switch for connecting a first electrode of the pumping capacitor to a first power source, a second switch for connecting the first electrode to an output node of the precharge voltage generation circuit, a control circuit for controlling on/off of the first and second switches, and a precharge voltage pumping circuit for driving a second electrode of the pumping capacitor with a second control signal,

the second control signal rises during an activation period of a first control signal that is a bit line precharge starting signal to the precharge circuit, and

a voltage amplitude of the second control signal is substantially the same as a voltage amplitude of a signal in the logic circuit device.

43. A semiconductor device with a semiconductor memory device and a logic circuit device therein,

wherein the semiconductor memory device includes: a plurality of memory cells; paired bit lines connected to the plurality of memory cells; a plurality of precharge circuits for precharging the paired bit lines to a predetermined precharge voltage in accordance with a first control signal; and a bit line precharge voltage generation unit for supplying a voltage for precharging to the plurality of precharge circuits, an equalizing voltage of the paired bit lines being different from the precharge voltage,

the bit line precharge voltage generation unit includes:

a precharge voltage generation circuit for generating the precharge voltage and supplying the precharge voltage to the plurality of precharge circuits; and

a precharge voltage pumping circuit including a pumping capacitor, a first switch for connecting a first electrode of the pumping capacitor to a first power source, a second switch for connecting the first electrode to an output node of the precharge voltage generation circuit, a control circuit for controlling on/off of the first and second switches, and a precharge voltage pumping circuit for driving a second electrode of the pumping capacitor with a second control signal,

the second control signal rises with a transition time longer than a transition time of the first control signal, after a predetermined delay time from activation of the first control signal that is a bit line precharge signal to the precharge circuit, and

a voltage amplitude of the second control signal is substantially the same as a voltage amplitude of a signal in the logic circuit device.